

貞方研究



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PEDOT:PSS

高温

低溫

電流



The figure illustrates a 4-input PLD architecture. On the left, a logic diagram shows two 2-input AND gates. The first AND gate has inputs A and B, and its output is S. The second AND gate has inputs A and B, and its output is C. Below the logic diagram is a truth table for the 4-input device:

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	0	0

On the right, a color-coded grid represents the device's internal structure. The grid is divided into columns labeled NOT, XNOR, NAND, and NOT, and rows labeled Vdd, S, and GND. Red lines connect the logic diagram to the grid.



電流

ベンタゼン

電圧

電流



1~6の有機デバイス関連は福田先生と共同で実施するテーマもあります。